Verilog-A Formulation of Godfrey-Lazzaro Model for Simulations in Cadence CAD System

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Abstract – **The simplified formulation of EKV compact model given by Godfrey and Lazzaro (GL model) is coded in Verilog-A HDL for circuit simulation in Cadence Design Framework. GL-model features an equation set incorporating explicit expression for the threshold voltage rather than the pinch-off voltage (inherent to the original EKV model). The model is verified against simulation results with the BSIM3v3 model embedded in a standard CMOS technology design kit.**

Keywords – **compact modeling, EKV, Godfrey-Lazzaro formulation, BSIM3v3, Verilog-A, circuit simulations.**

I. INTRODUCTION

Compact modeling of MOSFETs is a key milestone to efficiently achieving the analog design objectives. The demand for flexible, physics-based, full-featured state-of-the-art compact models has increased dramatically in the the sub-100 nm CMOS technology generations.

MOSFET compact models are coded in circuit simulators using general-purpose languages like C/C++, FORTRAN, etc. Accordingly, they are targeted specifically to the interface and internal data structures of their host simulator, and hence are inherently non-portable. In this context modification and optimization of a given model becomes a time-consuming and error-prone task.

An effective approach to overcome this gap between model development and its subsequent implementation in CAD tools is to formulate open source code models in analog HDLs such as Verilog-A/AMS or VHDL-AMS [1]. In the recent years Verilog-A has become increasingly viewed as most promising candidate for compact modeling purposes.

With this regard, the EKV MOSFET model is excellent example of a compact model that is appropriate for implementation in Verilog-A/AMS as it provides excellent tradeoff between accurate modeling results and small number of parameters. The original EKV model uses much fewer model parameters than the latest BSIM model versions [2].

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The present paper considers a basic approach to provide circuit designers with more faster and straightforward access to models in circuit simulators. That is, to choose the compact model for particular design needs and to code it into a hardware description language (HDL), and finally to embed it in a library of the CAD tool used in the design process.

We have coded in Verilog-A the Godfrey and Lazzaro formulation of the EKV model [5] with explicit formulation of the threshold voltage rather than the pinch-off voltage. The model was saved as a cellview in a Cadence library ready for use by circuit designers. Finally, the GL Verilog-A model predictions were compared against BSIM3v3 reference model from a technology design kit using Spectre simulator.

The original EKV model (Enz, Krummenacher, and Vittoz) is described in detail in [3] and its version EKV v2.6 (Bucher, Lallement, Enz, Théodoloz, Krummenacher) is described in [4]. Despite small number of parameters in EKV v2.6, it still remains fairly complex. That is why we take the simplified version of the model set forth by Godfrey and Lazzaro in [5]. The latter model (it is based on the Vittoz-Oguey approximation for obtaining a single expression for the drain current) offers simpler treatment of the EKV modeling methodology while retaining its applicability for circuit simulations.

II. GODFREY-LAZZARO MODEL

The Godfrey and Lazzaro present a simplification of the original EKV model that is quite useful in quick estimation of circuit/system performance or for long-channel devices (down to 0.7 μm) in contrast to the complex and time-consuming evaluation with full-featured EKV v2.6 or v3.0. In addition, compared to the original EKV model, the Godfrey-Lazzaro (GL) formulation accounts for short channel effects (e.g. channel length modulation) without introducing recurrent relations for calculation of its respective values. For example, in EKV v2.6 one needs to know the previous value of the forward current IF to calculate the CLM correction to the drain current which is not the case in the GL equation set.

Below we sketch the model equations of the Godfrey-Lazzaro formulation that are input in our in Verilog-A code.

A. Drain Current Smoothing Function

For MOSFETs in strong inversion the channel current is a quadratic function while for MOSFETs in weak inversion the channel current is an exponential function. Vittoz and

Oguey suggest a formula for the MOSFET channel current that interpolates (smoothes) these separate expressions [5].

$$F(x)=\ln^2\left(1+e^{x/2}\right)=\begin{cases}(x/2)^2 & , \ x>>0\\ e^x & , \ x<<0\end{cases} \quad (1)$$

This function smoothly interpolates between the quadratic and exponential operational regimes and allows expressing the MOSFET behavior in the otherwise difficult case of moderate inversion. The EKV model is based on the same interpolation approach as well. This is a mathematical trick and it is not really physically motivated.

Using the smoothing function (1) the channel current for the MOSFET takes the form

$$I_D=\frac{2\beta U_T^2}{\kappa}(I_F-I_R)(1+\lambda_c\ V_{DS}) \quad (2)$$

where λ_c is the parameter of channel length modulation, β is the transfer parameter, U_T is the thermal voltage — $U_T = kT/q$ (0.026 V at 300° K). The forward current and the reverse current are, respectively, given with

$$I_F=\ln^2\left[1+\exp\{U_1\left[\kappa(V_G-V_{Th})-V_S\right]\}\right] \quad (3)$$

$$I_R=\ln^2\left[1+\exp\{U_1\left[\kappa(V_G-V_{Th})-V_D\right]\}\right] \quad (4)$$

B. Threshold Voltage

What differs most in the Godfrey-Lazzaro formulation compared to the well-recognized EKV model is that Godfrey and Lazzaro use explicit formulation of the threshold voltage while the EKV uses explicit formulation of the pinch-off voltage.

The threshold voltage is

$$V_{Th}=\begin{cases}V_{FB}+|\phi_b|+\gamma\sqrt{|\phi_b|-(V_B-V_S)} & ,\mathrm{NMOS}(V_{BS}\le 0)\\ V_{FB}-|\phi_b|-\gamma\sqrt{|\phi_b|-(V_B-V_S)} & ,\mathrm{PMOS}(V_{BS}\ge 0)\end{cases} \quad (5)$$

The flat band voltage is given by

$$V_{FB}=\phi_{ms}-\frac{Q_{ss}}{C_{ox}} \quad (6)$$

ϕ_{ms} – silicon-oxide interface charge, Q_{ss} – fixed oxide charge, $\varepsilon_{Si} = 11.7\varepsilon_0$.

The Fermi potential (NA – the doping concentration) is

$$\phi_b=2\phi_F=2U_T\ \ln\frac{N_A}{n_i} \quad (7)$$

The body effect coefficient is

$$\gamma=\frac{1}{C_{ox}}\sqrt{2\times10^6\,\varepsilon_{Si}\,\rho} \quad (8)$$

The intrinsic carrier concentration is

$$n_i=1.64\times10^{15}T^{1.706}e^{-\frac{E_g}{2kT}} \quad (9)$$

for which the band gap is given with

$$E_g=\begin{cases}q\left(1.7+1.059\times10^{5}T-6.05\times10^{-7}T^2\right), & 0<T\le150\\ q\left(1.785+9.025\times10^{5}T-3.5\times10^{-7}T^2\right), & 150<T\le300\end{cases} \quad (10)$$

C. Additional Parameters

The remaining model parameters in the GL model are given below. The transfer parameter (appearing in (2))

$$\beta=10^{-4}\mu C_{ox}\frac{W}{L} \quad (11)$$

is temperature dependent. Its temperature dependence arises from the dependence on temperature of the mobility $\mu = \mu$ (T).

In the above equations $C_{ox} = q_{ox}/t_{ox}$ and

$$\kappa=\frac{C_{ox}}{C_{ox}+C_{dep}} \quad (12)$$

where $C_{dep} = \sqrt{10^6\rho\varepsilon_{Si}/2\phi_s}$ is the depletion capacitance which is a function of the surface potential ϕ_s:

$$\phi_s=\begin{cases}0.1\phi_b & ,\ \phi_{s1}<0.1\phi_b\\ \phi_{s1} & ,\ \phi_{s1}\ge0.1\phi_b\end{cases} \quad (13)$$

In (13)

$$\phi_{s1}=\phi_b\ \tanh\frac{V_G-V_{FB}-V_B+V_S}{V_{Th}} \quad (14)$$

D. Fitting Parameters

There are a number of geometric and physical parameters which affect device behavior. Some of them, such as oxide thickness (t_{ox}), are precisely defined, while others such as threshold voltage (V_{Th}) are poorly defined and difficult to measure. Many of these parameters play a minor or indirect role in device behavior from a circuit simulation standpoint. There are three parameters which are independent in process terms and which play key role in our model. These are: Q_{ss} – the channel charge due to surface states, N_a, substrate doping concentration, and μ_0, carrier mobility. Thus, these are used to “adjust" the model to achieve the expected behavior (results) for specific technologies and specific fabrication runs.

An overall advantage of the GL model is that the physical parameters are reasonably independent of each other and therefore can be separately adjusted to reflect and fit the device physical behaviors. This enables the designer to experiment with circuit behavior as a function of changes observed in physical parameter values, and associate this with feasible device fabrication processes.

III. Model Implementation in Verilog-A

The equations of the GL model are coded in Verilog-A. Next, a cellview is created in the libraries of Cadence

Design Framework. Below we provide the GL model Verilog-A code with minor abridgements.

```
module ekv_GL(d,g,s,b);

// EKV model in Godfrey-Lazzaro formulation

// // Node definitions //

inout d,g,s,b;            // external nodes
electrical d,g,s,b;       // external nodes


// // Model parameter definitions //

parameter real L = 0.7E-6 from[0.0:inf];
parameter real W = 20E-6 from[0.0:inf];

// // Local variables //

real Vg, Vs,Vb, Vd, VGprime, VP, Vds, Vbs, Vdb,
Ve;
real beta, n, kappa, Vp, Vt, Cdep, gamma, Vt0, V0,
phi_s, ni, lambda_c, Na, MU0, T, mu,k1, U1;
real Iff, Ir, Ispec, Id, Idsi, Ids;

// // Physical Constants //

real phi_f, phi_b, Eg;
real k, q, e_v, e_s, e_ox, Ut;


// Technology (Model) Parameters //

real rho, PHI_ms, QSS, Cox, Vfb, dNa, NaL, dMU0,
TOX, Early_s, L_0;

analog begin

Vg = V(g); Vs = V(s); Vd = V(d); Vb = V(b);

Vds = Vd - Vs; Vbs = Vb - Vs; Vdb = Vd - Vb;

// bulk doping conc [cm E-3](SPICE Level-2 NSUB)
Na = 2.4e17*dNa*(1 - NaL*L);

// carrier mobility (SPICE Level-2 u0) [cm^2/(V
s)] at 300 K
MU0 = 686.6*dMU0;


Cox =e_ox/TOX;                    // [F/m^2]
Vfb = PHI_ms - QSS/Cox;

// // Empirical Equations: // //

// // Temperature dependence of band gap (Eg) :

Eg = (1.1785 - 9.025e-5*T - 3.05E-7*T*T)*q;
   //for 150 < T < 300K end;

ni = 1.640E+15*pow(T,1.706)*exp(-Eg/(2*k*T));
   // 9.8929e+009 at T=300 [cm^-3];

phi_f = Ut*log(Na/ni);
phi_b = 2*phi_f;

lambda_c = 1*Early_s*1/(Ve + L - L_0);

// // Threshold voltage:  //

Vt = Vfb + abs(phi_b) + gamma*sqrt(abs(phi_b) -
Vbs);

Cdep = sqrt(rho*e_s*1e6*1/(2.0*phi_s));
kappa = Cox*1/(Cox + Cdep);

// // Intermediate expressions:  //

k1 = 2*beta*(Ut*Ut)*1/kappa;
U1 = 1/(2*Ut);

// // Model equations:  drain current //

Iff = (log(1 + exp(U1*(kappa*(Vg - Vt) -
Vs))))*(log(1 + exp(U1*(kappa*(Vg - Vt)- Vs))));
Ir = (log(1 + exp(U1*(kappa*(Vg - Vt) -
Vd))))*(log(1 + exp(U1*(kappa*(Vg - Vt) - Vd))));
Idsi = (Iff - Ir);
Ids = k1*Idsi*(1 + lambda_c*Vds);

I(d,s) <+ Ids;

end

endmodule
```

IV. SIMULATION RESULTS

We simulate a N-channel MOSFET with L = 0.7 μm and W = 20 μm. The parameter used in the GL model [5] and their values in our implementation are presented in Table 1.

TABLE 1. MODEL PARAMETERS

Parameter	Optimal value	Description
TOX (t_{ox})	$216{\times}10^{-10}$ [m]	Oxide thickness
PHI_ms (ϕ_{ms})	– 0.3 [–]	Silicon oxide interface charge
Early_s ($Early_s$)	0.12 [–]	Slope of Early effect
L_0 (L_0)	0.1 [–]	Intercept of Early effect
QSS (Q_{ss})	5.5×10^{-4} [C]	Fixed oxide charge
dNa (ΔNa)	1.0 [–]	Fitting parameter for the bulk doping Na
NaL (Na_L)	0.0 [cm^{-3}]	Effective doping concentration as a function of L
dMU0 ($\Delta\mu_0$)	1.0 [–]	Fitting parameter for the mobility μ_0 ($\mu_0 = 686.6\ \Delta\mu_0$)

In the figures below we present simulation results obtained by our Verilog-A implementation of the Godfrey-Lazzaro model as a standard Verilog-A cell in Cadence. The BSIM3v3 reference results are obtained in Cadence Spectre simulator for a standard 0.35 μm CMOS technology with gate length of 0.7 μm. Output and transfer characteristics as well as transconductances are presented in Figure 1, 2, and 3.

The comparison of results is done by simulating the standard design kit transistor (BSIM3v3) together with out Verilog-A transistor (GL-model). All characteristics have been obtained using a single parameter set.

In the output characteristic (Figure 1) we observe very good agreement between BSIM3v3 reference and the Godfrey-Lazzaro characteristics. For gate voltages V_{gs} = 1, 1.5, and 2 V the characteristics of the two models are almost identical; for V_{gs} = 0.5 and 2.5V we have notable discrepancy between BSIM3v3 reference and the GL simulation. This is most probably due to the fact that we use measurement data for a 0.7 μm device and simulate it using parameter set within a 0.35 μm technology design kit. Another reason for this discrepancy is the simplification of the GL model, which employs less number of model parameters in the equations compared to BSIM3 model.

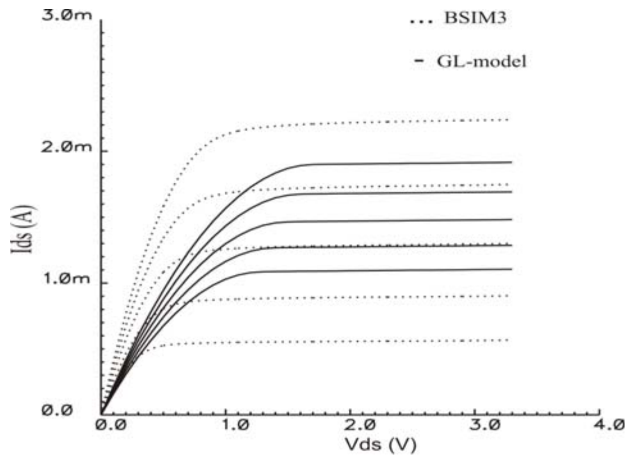

FIGURE 1. OUTPUT CHARACTERISTICS *IDS(VDS)*.

In the transconductance characteristics (Figure 2) the agreement between BSIM3 and Godfrey-Lazzaro model is worse, which is expected since these are second order characteristics.

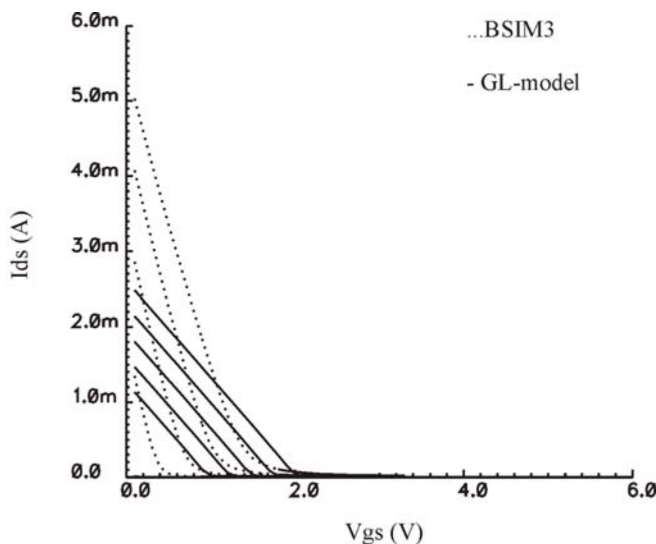

FIGURE 2. TRANSCONDUCTANCE CHARACTERISTICS *gmd = dIDS/dVDS(VDS) @ VGS* = (0, 2.5) V.

In the transfer characteristics (Figure 3) the agreement between BSIM3 and Godfrey-Lazzaro EKV implementation is also good.

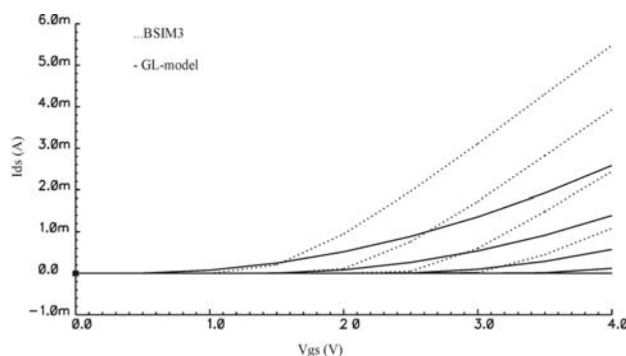

FIGURE 3. TRANSFER CHARACTERISTICS *IDS(VGS)*.

The results prove the usability of the presented method for open source code simulations. The fast and accurate simulations with accuracy comparable to commercial simulators show the practical applicability of the method to circuit-design and optimization purposes. The main advantages are that this method enables the user with flexibility in modeling giving direct access to model equations. It also ensures compatibility between different simulation platforms in CAD tools.

V. CONCLUSION

A simplified formulation of the EKV model proposed by Godfrey-Lazzaro is coded in Verilog-A HDL. This model is quite useful for general estimation of circuit performances, as opposed to the sophisticated and resource-consuming full-featured compact models.

On the other hand, the model realization represents a clear example of an all-purpose methodology for coding compact model equations in a portable, open source environment suitable for use in various simulation platforms. In practice, this proves to be a straightforward yet effective approach for circuit-level design purposes.

The simulation results with the GL model demonstrated good agreement with the reference BSIM3v3 results of a typical CMOS technology in the state-of-the-art Cadence CAD system. Both the straight and simple mathematical model structure and the efficient methodology for compact model implementation lead to real benefits for design community and academia.

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